PTO/SB/21 (08-03)

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10/735,123 Filing Date TRANSMITTAL **December 12, 2003** First Named Inventor **FORM** Igor KELLER Art Unit 2816 (to be used for all correspondence after initial filing) Examiner Name **Not Yet Assigned** 5 w/ 12 Attorney Docket Number Total Number of Pages in This Submission 188122000400 refs. ENCLOSURES (Check all that apply) After Allowance Communication Fee Transmittal Form Drawing(s) to Group Appeal Communication to Board of Fee Attached Licensing-related Papers Appeals and Interferences Appeal Communication to Group Petition Amendment/Reply (Appeal Notice, Brief, Reply Brief) Pétition to Convert to a After Final Proprietary Information **Provisional Application** Power of Attorney, Revocation Change of Correspondence Address Affidavits/declaration(s) Status Letter Other Enclosure(s) (please **Extension of Time Request Terminal Disclaimer** X identify below): 1. Copy of 12 Cited References **Express Abandonment Request** Request for Refund 2. Return Receipt Postcard **Information Disclosure Statement** CD, Number of CD(s) w/ Form PTO 1449 (4 pages) Certified Copy of Priority Document(s) Remarks Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53 SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Firm MORRISON & FOERSTER LLP (Customer No. 20872) Stephen C. Durant - 31,506 Individual name Signature Date 2004 July

I hereby certify that this correspondence	is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in
an envelope addressed to: Commissione	er for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on the date shown below.
Dated: <u>July 15, 200</u> 4	Signature: (Leah M. Kjellén)



CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, YA-22313-1450, paluly 15, 2004.

Leah M. Kjellén

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Igor KELLER et al.

Serial No.:

10/735,123

Filing Date:

December 12, 2003

For:

ROBUST CALCULATION OF CROSSTALK DELAY CHANGE IN INTEGRATED CIRCUIT DESIGN Examiner: Not Yet Assigned

Group Art Unit: 2816

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97 & 1.98

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, Applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO-1449. Copies of the documents are also submitted herewith. The Examiner is requested to make these documents of record.

	inis i	nformation Disclosure Statement is submitted:						
	With the application; accordingly, no fee or separate requirements are required.							
	Before	e the mailing of a first Office Action after the filing of a Request for Continued						
	Examination under § 1.114. However, if applicable, a certification under 37 C.F.R. §							
	1.97(e)(1) has been provided.							
\boxtimes	Within three months of the application filing date or before mailing of a first Office							
	Action on the merits; accordingly, no fee or separate requirements are required.							
	However, if applicable, a certification under 37 C.F.R. § 1.97(e)(1) has been provided.							
	After receipt of a first Office Action on the merits but before mailing of a final Office							
	Action or Notice of Allowance.							
		A fee is required. A check in the amount of is enclosed.						
		A fee is required. Accordingly, a Fee Transmittal form (PTO/SB/17) is attached						
		to this submission in duplicate.						
		A Certification under 37 C.F.R. § 1.97(e) is provided above; accordingly; no fee						
		is believed to be due.						
	After mailing of a final Office Action or Notice of Allowance, but before payment of the							
	issue fee.							
		A Certification under 37 C.F.R. § 1.97(e) is provided above and a check in the						
		amount of is enclosed.						
		A Certification under 37 C.F.R. § 1.97(e) is provided above and a Fee Transmittal						
		form (PTO/SB/17 is attached to this submission in duplicate.)						

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement under 37 C.F.R. § 1.97 and § 1.98 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the unlikely event that the transmittal form is separated from this document and the Patent Office determines that an extension and/or other relief (such as payment of a fee under 37 C.F.R. §1.17(p)) is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing **188122000400**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: July 14, 2004

Respectfully submitted,

Stephen C. Durant

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Form PTO-1449					Docket Number 188122000400		Application Number 10/735,123				
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	IN AN APPLICATION				Igor KELLER et al.						
(Use several sheets if necessary)					Filing Date December 12, 2003 Group Art Unit 2816						
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	1.	R. Arunacha	lam et al., "TACO: T	imin	g Analysis With	COupling", AC	CM 2000, 4 pg	gs.			
	2.		l., "Miller Factor for Con Computer Aided D			Delay Calculat	ion", IEEE, Ir	nternationa	al		
	3.	 J. F. Croix et al., "Blade and Razor: Cell and Interconnect Delay Analysis Using Current-Based Models", DAC June 2-6, 2003, Anaheim CA, pp. 386-389. F. Dartu et al., "Calculating Worst-Case Gate Delay Due to Dominant Capacitance Coupling", DA 97, Anaheim CA, 6 pgs. 									
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6. I. Keller et al., "A robust cell-level crosstalk delay change analysis", 8 pgs. 7. I. Keller et al., "On a robust noise-on-delay cell-level analysis", 7 pgs.											
	8. A. Odabasioglu et al., "PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 17, no.8, At 1998, pgs. 645-654.										
	9.	9. V. Raghavan et al., "AWESpice: A General Tool for the Accurate and Efficient Simulation of Interconnect Problems", 29th ACM/IEEE Design Automation Conference, paper 6.3, 1992, pgs. 87-92.									
	10.										
	11.										
12. V. Zolotov et al., "Noise Propagation and Failure Criteria for VLSI Designs", IEEE 2002, 8 pgs.											
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